CLAIMS:

1. A data carrier (1) for the storage of data,
which data carrier (1) has a first interface (10) for communication with a first communication device (2) and
which data carrier (1) has a second interface (25) for communication with a second communication device (3) and
which data carrier (1) includes an electrical circuit arrangement (12),
which circuit arrangement (12) includes circuit parts (13, 14, 15) of the first interface (10) and circuit parts (27, 28, 29) of the second interface (25) and
which circuit arrangement (12) has memory means (17) for the storage of data, which memory means (17) has a first storage location (22) and a second storage location (23), and
which circuit arrangement (12) has a first memory access means (18), arranged between the first interface (10) and the memory means (17), for accessing the memory means (17) and
which circuit arrangement (12) has a second memory access means (33), arranged between the second interface (25) and the memory means (17), for accessing the memory means (17) and
which circuit arrangement (12) has access enabling means (21, 37, 39, 19) which enable the first storage location (22) to be accessed only by the first memory access means (18), characterized
in that the data carrier (1) has additional memory access means (38) adapted to cooperate with the second memory access means (33) and adapted to access the first storage location (22) and designed to verify an access authorization for the access to the first storage location (22), and
in that after a positive result of the verification of the access authorization the second memory access means (33) can, in addition, access the first storage location (22) via the additional memory access means (38) and via the first memory access means (18).

2. A data carrier (1) as claimed in Claim 1, characterized
in that the additional memory access means (38) are included in the first memory access means (18).

3. A data carrier (1) as claimed in Claim 1, characterized in that the additional memory access means (38) include access code verification means (40) for the verification of an access code (ZC1), and in that a first access code (ZC1) from the second memory access means (33) as well as a second access code (ZC2) can be applied to the access code verification means (40), which second access code can be calculated from data stored in the first storage location (22), and in that agreement of the first access code (ZC1) and the second access code (ZC2) is prerequisite for the positive result of the verification of the access authorization.

4. A data carrier (1) as claimed in Claim 3, characterized in that an access code calculation means (42) has been provided for the calculation of the calculable second access code (ZC2), and in that the access code calculation means (42) is adapted to execute a triple DES encryption process.

5. A data carrier (1) as claimed in Claim 3, characterized in that the additional memory access means (38) have, in addition to the access code verification means (40), access condition verification means (43) for the verification of an access condition (ZB1), and in that a first access condition (ZB1) from the second memory access means (33) as well as a second access condition (ZB2) can be applied to the access condition verification means (43), which second access condition can be determined from data stored in the first storage location (22), and in that agreement of the first access code (ZC1) and the second access code (ZC2) as well as agreement of the first access condition (ZB1) and the second access condition (ZB2) are prerequisite for the positive result of the verification of the access authorization.

6. A data carrier (1) as claimed in Claim 1, characterized in that the electrical circuit arrangement (12) of the data carrier (1) takes the form of an integrated circuit.

7. An electrical circuit arrangement (12) for a data carrier (1) for the storage of data,

which circuit arrangement (12) includes circuit parts (13, 14, 15) of a first interface for communication with a first communication device (2) and

which circuit arrangement (12) includes circuit parts (27, 28, 29) of a second interface (25) for communication with a second communication device (3) and

which circuit arrangement (12) has memory means (17) for the storage of data, which memory means (17) has a first storage location (22) and a second storage location (23), and

which circuit arrangement (12) has a first memory access means (18), arranged between the circuit parts (13, 14, 15) of the first interface (10) and the memory means (17), for accessing the memory means (17) and

which circuit arrangement (12) has a second memory access means (33), arranged between the circuit parts (27, 28, 29) of the second interface (25) and the memory means (17), for accessing the memory means (17) and

which circuit arrangement (12) has access enabling means (21, 37, 39, 19) which enable the first storage location (22) to be accessed only by the first memory access means (18),

characterized

in that the circuit arrangement (12) has additional memory access means (38) adapted to cooperate with the second memory access means (33) and adapted to access the first storage location (22) and designed to verify an access authorization for the access to the first storage location (22), and

in that after a positive result of the verification of the access authorization the second memory access means (33) can, in addition, access the first storage location (22) via the additional memory access means (38) and via the first memory access means (18).

8. A circuit arrangement (12) as claimed in Claim 7, characterized

in that the additional memory access means (38) are included in the first memory access means (18).

9. A circuit arrangement (12) as claimed in Claim 7, characterized

in that the additional memory access means (38) include access code verification means (40) for the verification of an access code (ZC1), and

in that a first access code (ZC1) from the second memory access means (33) as well as a second access code (ZC2) can be applied to the access code verification means (40), which second access code can be calculated from data stored in the first storage location (22), and

in that agreement of the first access code (ZC1) and the second access code (ZC2) is prerequisite for the positive result of the verification of the access authorization.

10. A circuit arrangement (12) as claimed in Claim 9, characterized in that an access code calculation means (42) has been provided for the calculation of the calculable second access code (ZC2), and
in that the access code calculation means (42) is adapted to execute a triple DES encryption process.

11. A circuit arrangement (12) as claimed in Claim 9, characterized
in that the additional memory access means (38) have, in addition to the access code verification means (40), access condition verification means (43) for the verification of an access condition (ZB1), and
in that a first access condition (ZB1) from the second memory access means (33) as well as a second access condition (ZB2) can be applied to the access condition verification means (43), which second access condition can be determined from data stored in the first storage location (22), and
in that agreement of the first access code (ZC1) and the second access code (ZC2) as well as agreement of the first access condition (ZB1) and the second access condition (ZB2) are prerequisite for the positive result of the verification of the access authorization.

12. A circuit arrangement (12) as claimed in Claim 7, characterized
in that the electrical circuit arrangement (12) takes the form of an integrated circuit.

13. A method (44) of accessing memory means (17) of a data carrier (1) having a first storage location (22) and a second storage location (23), the method (44) comprising the steps defined hereinafter, namely
storing data in at least the first storage location (22) of the memory means (17),
enabling the first storage location (22) to be accessed only by the first memory access means (18),
characterized
in that access authorizations for access to the first storage location (22) are applied to additional memory access means (38), and

in that the applied access authorizations are verified with the aid of the additional memory access means (38), and

in that after verification of the access authorizations and in the case of a positive result of the verification the first storage location (22) is accessed additionally by a second memory access means (33) via the additional memory access means (38) and via the first memory access means (18).

14. A method (44) as claimed in Claim 13, characterized

in that during the verification of the access authorizations a first access code (ZC1) is compared with a second access code (ZC2) by means of access code verification means (40), and

in that the first access code (ZC1) is applied from the second memory access means (33), and the second access code (ZC2) is calculated from data stored in the first storage location (22), and

in that agreement of the first access code (ZC1) and the second access code (ZC2) is prerequisite for the positive result of the verification.

15. A method (44) as claimed in Claim 14, characterized

in that during the verification of the access authorizations, in addition to the comparison of the first access code (ZC1) and the second access code (ZC2) with the aid of the access code verification means (40), a first access condition (ZB1) is compared with a second access condition (ZB2) with the aid of access condition verification means (43), and

in that the first access condition (ZB1) is applied from the second memory access means (33) to the access condition verification means (43) and the second access condition (ZB1) is determined from data stored in the first storage location (22), and

in that agreement of the first access code (ZC1) and the second access code (ZC2) as well as agreement of the first access condition (ZB1) and the second access condition (ZB2) are prerequisite for the positive result of the verification.